HIGH GAIN TWO-STAGE CLASS-AB OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

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ABSTRACT
A new two-stage class-AB operational transconductance amplifier that is suitable for analog-to-digital converters (ADC) and switched capacitor (SC) filters is presented. The proposed design is based on adaptive biasing at the input stage, cascoding and class-AB output stage techniques. The OTA have been designed in 0.18 µm CMOS technology with simulation results showing gain and gain bandwidth improvements of 201% and 12% respectively when compared to a conventional Class-AB OTA. The circuit is operated at 1.8V supply voltage.

Keywords:
Integrated circuits, analog CMOS circuits, amplifiers, two-stage, class-AB, adaptive biasing, high gain, gain bandwidth, operational transconductance amplifier (OTA).

INTRODUCTION

Nowadays, CMOS Operational Transconductance Amplifier (OTA) is one of the most used and a crucial building block in analog circuit application (Nguyen & Lee, 2006), used in applications like switched-capacitor filters, continuous-time filters and high-speed A/D converter circuits (Lopez-Martin, Baswa, Ramirez-Angulo, & Carvajal, 2005) (Rambabu, Majumder, & Mondal, 2017). OTA has a very high output impedance; hence, OTA is best defined in terms of transconductance (Parveen, 2013). The ability of the operational transconductance amplifier to operate in both voltage and current mode, enables diversity in circuit design (Lim, 2000).

The advancements achieved in MOS technology have resulted in downscaling the dimensions of the transistors, leading to reduced intrinsic voltage gain. As a result, the upper limit of the open-loop gain achievable by OTA is reduced. Moreover, low gain OTAs have direct effect on the accuracy of systems such as analog to digital converters (ADC) and switched capacitor circuits (Yang & Roberts, 2016) (S. I. Singh, 2017). To achieve higher gain, employing class-AB at the second stage of the OTA can result in larger gain bandwidth due to higher output voltage swing, which can't be achieved using a class-A output stage due to its characteristics (Nur, Baharudin, Jambek, & Ismail, 2014) (Noormohammadi, Lazarjan, & HajSadeghi, 2012).

TWO-STAGE CLASS-AB OTA

Proposed OTA is designed based on adaptive biasing and current boosting techniques. It consists of three main OTA techniques in OTA design which are adaptive biasing at the input stage, push-pull amplifier at the output stage and cascoding. For the input stage, it consists of two input matched transistors M1 and M2 cross coupled with two level shifters. Furthermore, each one of the level shifters is made of two flipped voltage followers (FVF) consisting of transistors M5, M6, M7 and M8 and two current source transistors M9 and M10. Further, when there is a large differential input signal applied, the current delivered becomes much larger than the quiescent current. therefore, this technique uses class-AB operation which makes it preferable in low power devices. Adaptive biasing technique prevents settling time limitations by slew rate and improves small signal characteristics

such as gain-bandwidth product and achieving near optimal current efficiency without increasing the power consumption (Galan et al., 2007).

Additionally, the proposed OTA design has a class-AB output stage that consists of a common source amplifier or push-pull consisting of transistors M17, M18, M25 and M26. Class-AB at the output maintains a low quiescent current and improve the slew rate as well as generating the maximum output current (Kim et al., 2009) (Nur et al., 2014).

The third main building technique in the proposed design is cascode amplifier consisting of transistors M19, M20, M21, M22, M23 and M24 where three transistors are cascoded in each side of the proposed OTA. Further, cascoding increases the frequency response due to its ability to reduce the input capacitance. On the other hand, this configuration requires additional headroom voltage where the minimum output voltage of a triple cascode is equal to the sum of three overdrive voltages which makes it unsuitable for low voltage applications. Also, this configuration increases the output impedance which causes voltage gain reduction when the output voltage is maximized (Razavi, 2016).

The signal through the OTA starts flowing in the input stage at transistors M1 and M2 then flows to adaptive biasing circuit that is part of the input stage. Further, the signal flows to the flipped voltage follower (FVF) and then to the cascode amplifier and ends up at the push-pull amplifier at the output stage.

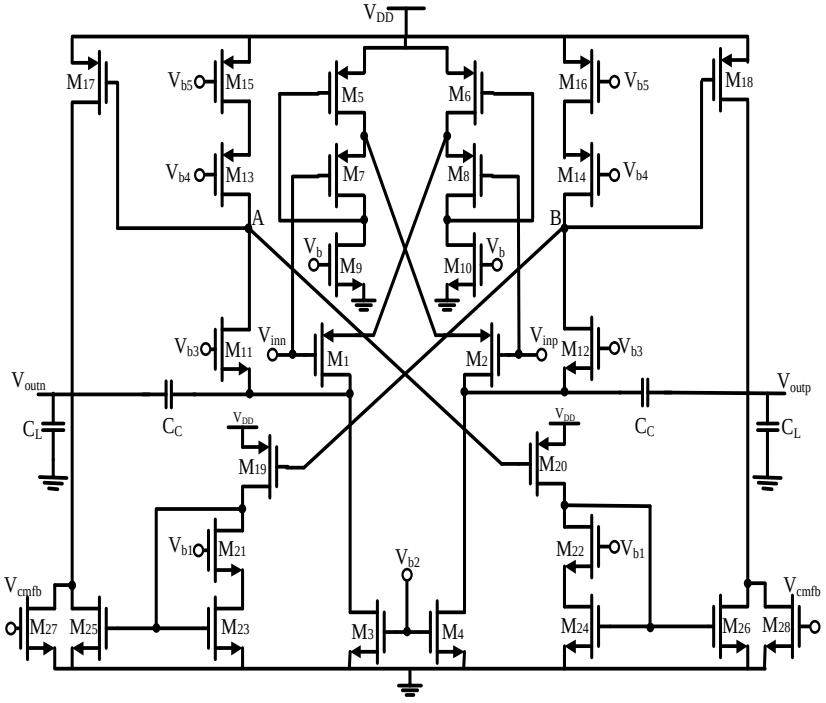

Figure 1: Two-Stage Class-AB OTA

The DC gain of each stage of the two-stage class-AB OTA is calculated through the impedance and transconductance produced by each transistor on the input and the output path considering the type of amplifier created by the CMOS devices arrangement such as common source amplifier, common gate amplifier, cascode amplifier and push-pull amplifier. The gain of an OTA is the ratio of output signal to input signal given as:

$$A_V = \frac{V_{outp} - V_{outn}}{V_{inp} - V_{inn}} \tag{1}$$

Due to transistors' matching, the transconductance and the resistance of transistors on the opposing sides are the same. Therefore:

$$A = \frac{V_{outp} - V_{outn}}{V_{in}} = \frac{g_{m2}\left(r_{o2} // r_{o4}\right) \cdot r_{o12} \cdot \left(g_{m19} r_{o19} // g_{m21} r_{o21} r_{o23}\right) \cdot g_{m19} r_{o19} \cdot g_{m18} g_{m26}\left(r_{o18} // r_{o26}\right)}{1 / g_{m2}} \tag{2}$$

Generally, two-stage amplifiers are unable to achieve such stability without a compensation method because the architecture causes two pole phase margin. Moreover, each pole contributes to a 90 degrees of phase margin degradation where if both dominant and non-dominant pole fall inside the range unity gain frequency, the amplifier destabilizes and oscillates. Therefore, a functional method to improve the OTA's stability is Miller compensation which adds a compensation capacitor from the input stage to the output stage. Also, the compensation works to move the dominant pole closer, and the non-dominant pole away from the unity-gain frequency which if it falls in that range results in destabilization of the OTA. Therefore, the dominant pole can be expressed as:

$$P_1 = -\frac{1}{\left(r_{o1} // r_{o3}\right) \cdot C_C} \tag{3}$$

Whereas, the non-dominant pole can be expressed as:

$$P_2 = \frac{1}{\left(1 / g_{m25}\right) \cdot C_L} \tag{4}$$

SIMULATION RESULTS

The two-stage class-AB OTA was designed using Silterra 0.18 µm standard CMOS technology with a supply voltage of 1.8 V and load capacitance 1pF with a threshold voltage for NMOS and PMOS of 0.45 V. Also, a comparison is provided with other OTA techniques. Figure 2 shows the gain of the two-stage class-AB OTA in comparison with other topologies and the advantage the proposed OTA has over other designs in terms of gain.

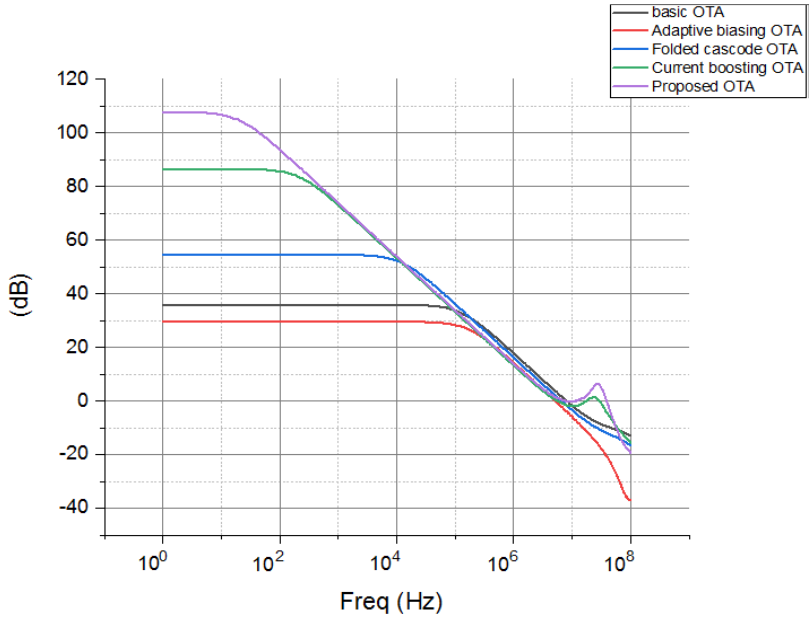

Figure 2: Gain

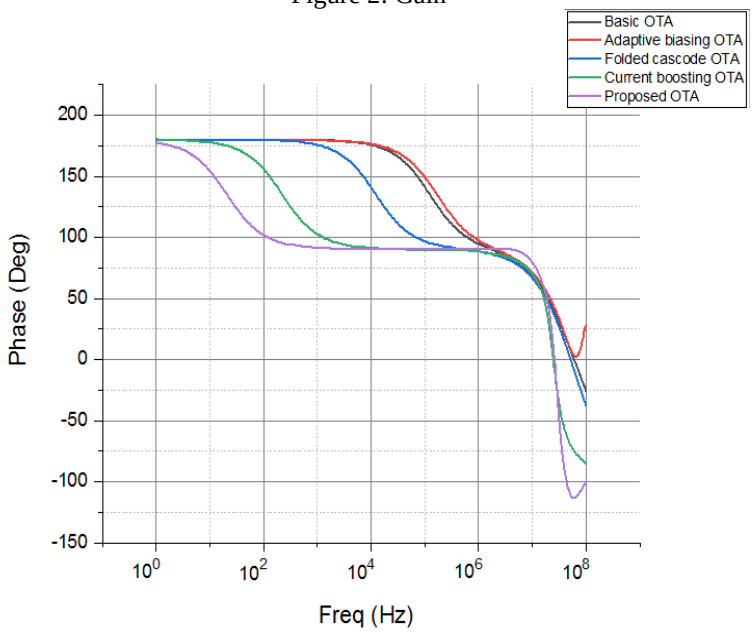

Figure 3: Phase

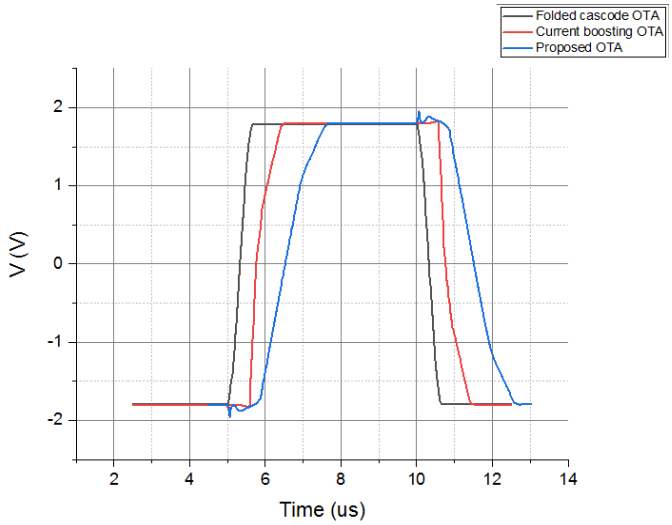

Figure 4: Transient Response

Figure 3, shows the phase margin of the proposed OTA against other topologies where it has the highest gain of 8.8 MHz and ha a stable operation with a phase margin greater than 60 degrees. Also, Figure 4 shows the slew rate where the proposed OTA slew rate suffers due to using a large compensation capacitor to achieve stability in the operation of the proposed OTA. Table 1 shows performance comparison between the proposed OTA and other topologies.

Table 1: Performance Comparison

OTA	**(林伸行, 2017)**	**(Galan et al., 2007)**	**(Rezaei & Ashtiani, 2008)**	**(Noormohammadi et al., 2012)**	**Proposed**
Power Supply	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
Technology	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm
Gain	35.7 dB	29.5 dB	55 dB	86 dB	107.5 dB
Bandwidth	125 KHz	174 KHz	9.3 KHz	221 Hz	20 Hz
GBW	7.9 MHz	5 MHz	6.6 MHz	5.6 MHz	8.8 MHz
Phase Margin	73 º	81 º	90 º	86 º	77 º
Slew Rate	94.9 V/µS	89.3 V/µS	7.3 V/µS	4.6 V/µS	2.4 V/µS
Power Dissipation	145 µW	142 µW	163 µW	175 µW	160 µW
C_L / **C_C**	1pF / 3pF	1pF / 1pF	1pF / 2pF	1pF / 4pF	1pF / 8pF
FOM	0.09	0.06	0.08	0.07	0.11

CONCLUSION

The proposed OTA was designed using Silterra 0.18-µm standard CMOS technology. Moreover, proposed OTA consists of three main techniques used in the design to improve the performance. The first technique the proposed OTA consists of is adaptive biasing at the input stage to increase the input impedance and improve the DC gain. Then, push-pull amplifier at the output stage which maintains low quiescent current and improves the slew rate. Furthermore, cascoding technique that

improves the frequency response. The techniques used also improved the gain bandwidth of the proposed OTA as they improve small signal characteristics. As a result, the proposed OTA achieved a gain of 107.5 dB and a gain bandwidth of 8.8 MHz where it can be used in high precision application such analog-to-digital converters and high-performance switched capacitor filters. Further, RC miller compensation was used to achieve a stable operation in the proposed OTA with a phase margin of 77 degrees.

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